IN THE SPECIFICATION:

1. On page 1, alter the paragraph beginning at line 1 as:

Cross References to Related Applications

This application ~~claims priority to~~ is a continuation in part of U.S. Regular Patent Application Serial No. 10/731,803 filed December 9, 2003~~,~~ and is a continuation in part of U.S. Regular Patent Application Serial No. 10/731,804, filed December 9, 2003, both of which claim priority to U.S. Provisional Patent Application Serial No. 60/431,940, filed December 9, 2002, and to U.S. Provisional Patent Application Serial No. 60/478,922, filed June 16, 2003, all of which are incorporated herein by reference for all purposes.

2. On page 3, alter the paragraph beginning at line 12 as:

In order for EDGE to provide increased data rates within a 200 ~~KHz~~ kHz GSM channel, it employs a higher order modulation, 8-PSK (octal phase shift keying), in addition to GSM's standard Gaussian Minimum Shift Keying (GMSK) modulation. EDGE allows for nine different (autonomously and rapidly selectable) air interface formats, known as Modulation and Coding schemes (MCSs), with varying degrees of error control protection. Low MCS modes, (MCS 1-4) use GMSK (low data rate) while high MCS modes (MCS 5-9) use 8-PSK (high data rate) modulation for over the air transmissions, depending upon the instantaneous demands of the application and the operating conditions.

3. On page 11, alter the paragraph beginning at line 11 as:

FIG. 3 is a block diagram illustrating in more detail the wireless terminal of FIG. 2, with particular emphasis on the digital processing components of the wireless terminal. The digital

processing components 204 include a system processor 302, a baseband processor 304, and a plurality of supporting components. The supporting components include an external memory interface 306, Multi Media Interface (MMI) drivers and I/F 308, a video I/F 310, an audio I/F 312, Hands Fee I/F 338, a voice band CODEC 314, auxiliary functions 316, a modulator/demodulator 322, ROM 324, RAM 326 and a plurality of processing modules. In some embodiments, the modulator/demodulator 322 is not a separate structural component with these functions being performed internal to the baseband processor 304.

4. On page 24, alter the paragraph beginning at line 1 as:

Next, the IR processing module 328 (or IR control process 332) determines whether the data block is an initial transmission of the RLC block or whether the data block is a retransmission of the RLC block (step ~~906~~ 908). Alternately, the IR processing module 328 may pass the decoded information back to the IR control process 332, which makes the determination regarding whether the data burst is a retransmission. This determination may be made by reading rtx, rtx1, and rtx2 from the Type I IR memory for the block sequence number of the data block, e.g., RLC block BSN. If this is a first transmission of the data block, e.g., rtx=0, then operation proceeds to step 910. If not, the data block is a retransmission of a previously transmitted data block, e.g., rtx>0 and operation proceeds to step 916.

5. On page 25, alter the paragraph beginning at line 21 as:

Referring particularly to FIG. 10, when storage of a data block is required, the IR control process 332 or IR processing module 328 determines whether Type II IR memory is available for the BSN (step 1002). If Type II IR memory is available for the BSN the IR control process 332

or IR processing module 328 stores the data block in a four bit format in Type II IR memory corresponding to the BSN (step 1004). The IR control process 332 or IR processing module 328 then updates the Type I IR memory for the BSN according to the data stored, i.e., update rtx, rtx1, or rtx2, mode (for the stored copy), MCS mode (for the stored copy), and Type II IR memory address (for the stored copy) (step 1006).